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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/629,780	07/31/2000	Yowjuang W. Liu	5251	4875

7590 10/21/2002

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EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	10

DATE MAILED: 10/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/629,780	LIU ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-18 and 20* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 5251

Filing Date: 7/31/2000

Claimed Foreign Priority Date: none

Applicant(s): Liu et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment (paper no.9) filed on 9/9/2002.

Acknowledgment

1. The amendment (paper no. 9) filed on 9/9/2002 in response to the Office action (paper no. 8) mailed on 6/5/2002 has been entered. The present Office action (paper no. 10) is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 16-20.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim (JP 8-274198).

4. Kim shows (see, *e.g.*, figs. 5-6) all aspects of the instant invention including a method for fabricating a semiconductor device with a trenched gate, said method comprising:

- etching a trench **49** having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate **41**
- forming a trench-to-gate insulating layer inside the trench **49**
- forming a trenched gate electrode **57** on the trench-to-gate insulating layer inside the trench **41**
- forming source/drain regions **45, 47** in the semiconductor substrate **41**
- forming an inter-gate dielectric layer **61** on a top surface of the trenched gate electrode **57**
- forming a control gate electrode **63** on a top surface of the inter-gate dielectric layer **61**

wherein

- the trench-to-gate insulating layer comprises:
  - a trench gate-dielectric spacer **52** formed on the upright vertical sidewalls inside the trench **49**
  - a trench gate tunneling dielectric **53** formed on the bottom surface inside the trench **49**
- the source and drain regions **45, 47** partially extend laterally underneath the bottom of the trench **49**

Claim Rejections - 35 USC § 103

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 5960284).

7. Regarding claim 17, Kim shows most aspects of the instant invention (see paragraph 4 above). In addition, Kim shows (see, *e.g.*, fig. 6h) the step of forming the trenched gate-electrode **57** comprising the step of depositing a layer of polysilicon on the trench-to-gate insulating layer inside the trench **49**. Kim, however, fails to show the step of forming the trenched gate-electrode also comprising the step of planarizing the layer of polysilicon to a substantially planar orientation with a top surface of the semiconductor substrate.

Lin (see, *e.g.*, figs. 7B and 8B), on the other hand, shows a step of forming a trenched gate-electrode comprising the step of planarizing the layer of polysilicon to a substantially planar orientation with a top surface of the semiconductor substrate. Because the floating gate is under the wafer surface, the profile of stacking the gate above the silicon surface is the same as that of the peripheral devices (col.6/ll.43-45). Therefore, the stacking gate etching can be done simultaneously with the control gate etching for peripheral devices (col.5/ll.45-47).

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have Kim's step of forming the trenched gate-electrode further comprising Lin's step of planarizing the layer of polysilicon to a substantially planar orientation with a top surface of the semiconductor substrate since this will provide for a reduction in the number of method steps by for example simultaneously etching the stacking gate of Kim and any peripheral devices.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 6127226) and Jaeger.

9. Regarding claim 18, Kim shows most aspects of the instant invention (see paragraph 4 above), except for a step of implanting the semiconductor substrate to form sidewall doping in the substrate laterally spacing each of the source and drain regions from the trench.

Lin, on the other hand, shows (see, e.*g.*, fig. 5B) a step of implanting a semiconductor substrate **12** forming sidewall dopings **22** in the substrate **12** and laterally spacing each of the source **34S** and drain **34D** regions from the trench (see, e.*g.*, fig. 9B). Moreover, Lin teaches that this step is a threshold implantation step (col.4/ll.65).

Jaeger (pp.178) teaches that the threshold voltage is directly related to the substrate doping and that there are several tradeoffs involved in the choice of substrate doping. According to Jaeger (pp.178), Lin's threshold implantation step is routinely used in the art to separate the threshold-voltage design from other factors involved in the choice of substrate doping.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to include in Kim's method the step suggested by Lin of implanting the semiconductor substrate forming sidewall dopings that laterally space each of the source and drain regions since, as taught by Jaeger, this is a step routinely used in the art to separate threshold voltage design considerations from other factors involved in the choice of substrate doping.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lin (US 6127226) and Jaeger, further in view of Wolf (US 3873371).

11. Regarding claim 20, Kim shows most aspects of the instant invention (see paragraph 4above), except for a step of implanting the semiconductor substrate to form sidewall doping in the substrate laterally spacing each of the source and drain regions from the trench.

Lin, on the other hand, shows (see, *e.g.*, fig. 5B) a step of implanting the semiconductor substrate **12** forming sidewall dopings **22** in the substrate **12** and laterally spacing each of the source **34S** and drain **34D** regions from the trench (see, *e.g.*, fig. 9B). Moreover, Lin teaches that this step is a threshold implantation step (col.4/ll.65)

Jaeger (pp.178) teaches that the threshold voltage is directly related to the substrate doping and that there are several tradeoffs involved in the choice of substrate doping. According to Jaeger (pp.178), Lin's threshold implantation step is routinely used in the art to separate the threshold-voltage design from other factors involved in the choice of substrate doping.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to include in Kim's method the step suggested by Lin of implanting the semiconductor substrate forming sidewall dopings that laterally space each of the source and drain regions since, as taught by Jaeger, this is a step routinely used in the art to separate threshold voltage design considerations from other factors involved in the choice of substrate doping.

In addition, Lin shows that the sidewall dopings are ion implanted at an angle to assure that the substrate sidewalls are implanted at the right dosage (see, *e.g.*, fig. 5B; col.4/ll.64-col.5/ll.3). Lin, however, fails to specify that the angle of implantation be approximately between 15-75°. Angle differences, however, are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes.

Wolf (col.2/ll.10-14), for example, teaches that the angle of implantation is a design variable that, if properly chosen, allows controlling the location at which the implanted impurities are introduced into the semiconductor substrate.

Accordingly, it would be an obvious matter of design choice to select a suitable angle for the ion implantation of Lin's sidewall dopings, as taught by Wolf, since the angle of implantation is a variable of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

Allowable Subject Matter

12. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

13. Applicant's arguments with respect to claims 16-18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814

~~Fax Center located in Crystal Plaza 4, room 3C23.~~ The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

18. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

19. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 438/257-267, 257/314-326	10/9/2002
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	10/9/2002

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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MDP/mdp
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